UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/826,986	04/05/2001	Bishop Chapman Brock	AUS920000853US1	4095

7590 05/05/2004

Kelly K. Kordzik
Suite 800
100 Congress Avenue
Austin, TX 78701

EXAMINER	
TRUJILLO, JAMES K	
ART UNIT	**PAPER NUMBER**
2116	3

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/826,986	Applicant(s) BROCK ET AL.	
	Examiner James K. Trujillo	Art Unit 2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 0501*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file:

2. Claims 1-33 are presented for examination.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore,

a. the "first receiving circuit", the "second receiving circuit", the "third circuit", the "fourth circuit" and the "fifth circuit" as per claims19 and dependents thereof;

b. the "cooling means" as per claims 4, 18, 21, 29 and 32 and any dependents thereof;

c. the "cooling fan" as per claims 5, 16, and 29;

d. the "thermo-electric cooler" as per claim 6;

e. the "chilled fluid and solid state cooling units"

must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to under 37 CFR 1.84 (o). Suitable descriptive legends may be required where necessary for understanding of the drawing. Therefore, figure 1 should have suitable legends for the block elements for understanding of the drawing.

Specification

5. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The specification disclose the following claimed elements.

a. the "thermo-electric cooler" as per claim 6.

b. the "chilled fluid" and "solid state" cooling units as per claim 23.

Claim Objections

6. Claim 15 is objected to because of the following informalities: the second recitation of "data defining a desired processor power consumption level" appears to be redundant and should be deleted. Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 19, 24 and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Kikinis, U.S. Patent 5,502,838.

9. As to claims 24, Kikinis taught a multiprocessor system comprising a plurality of processors and a controller for managing power and performances in said multiprocessor system, said controller comprising:

a. circuitry for receiving first sensor data defining physical parameters of said multiprocessor system (each processor has a temperature sensor which is sent to controller 65) [col. 5 lines 5-13];

b. circuitry for receiving first parameters corresponding to operational requirements (required voltage for a given clock rate) of said multiprocessor system [col. 5 lines 24-32];

c. circuitry for determining power and performance goal settings (for adjusting the voltage and clock) for processors in said multiprocessor system in response to said first sensor data and said first parameters (based on temperature and required voltage) [col. 5 lines 5-51];

d. circuitry for generating a set of controls for said multiprocessor system in response to said power and performance goal settings (the controller generates signal for voltage and clocks for the processors) [col. 5 lines 5-51];

e. circuitry for applying said set of controls to adjust operation parameters in said multiprocessor system (the controller actually adjusts the voltage and clock frequency of the processors accordingly) [col. 5 lines 5-51].

In summary, Kikinis teaches a multiprocessor system that has a controller which controls the voltage and frequency of each of the processors according to their respective temperatures.

10. As to claim 33, Kikinis taught the multiprocessor system according to claim 24, described above. Kikinis further teaches wherein said first parameters comprise policy of

operation parameters for said multiprocessor system (voltage and clock frequency must correspond for the processors to function properly).

11. As to claim 19, as set forth hereinabove Kikinis teaches circuitry:

a. operable to receive first sensor data corresponding to physical parameters of said multiprocessor system (each processor has a temperature sensor which is sent to controller 65) [col. 5 lines 5-13];

b. operable to receive first parameters defining operational requirements of said multiprocessor system [col. 5 lines 24-32];

c. operable to determine power and performance goal settings for said processors in said multiprocessor system in response to first data and first parameters [col. 5 lines 5-51];

d. operable to generate a set of controls for said multiprocessor system in response to said power and performance goal settings [col. 5 lines 5-51]; and

e. operable to apply said set of controls to adjust operation parameters of said processors in said multiprocessor system [col. 5 lines 5-51].

Because Kikinis teaches the claimed circuitry Kikinis inherently has the first and second receiving circuits as well as third, fourth and fifth circuits.

12. As to claim 1, Kikinis taught the claimed controller and system. Therefore he also taught the claimed method.

13. As to claim 11, Kikinis taught the method according to claim 1 described above. Kikinis further teaches wherein said first parameters comprise quality of service parameters for said multiprocessor system (control clock rate and shifting load management) [col. 5 lines 11-23].

Wherein controlling the clock rate affects quality of service because if the clock rate is reduced the service time increases for a particular task.

14. As to claim 12, Kikinis taught the method according to claim 1 as described above. Kikinis further teaches wherein the first parameters comprise policy of operation for said multiprocessor system [col. 5 lines 33-41]. Wherein adjusting the voltage would require that the frequency of operation be in accordance.

15. As to claim 13, Kikinis taught the method according to claim 11, as described above. Kikinis further teaches that quality of service parameters comprise assignment of data defining processor assignment to tasks performed by said multiprocessor system (task are inherently assigned to processors) [col. 1 lines 55-63], access availability for processors in said multiprocessor system (in shifting computational load access availability for processors must be determined), performance level data defining a performance for an application executing on processors of said multiprocessor system (clock rates are controlled according to heat generation in each sensed region) and processor operation data defining which of said processors are operational (shifting computational and logic load) [col. 5 lines 5-23].

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikinis.

18. As to claim 25, Kikinis taught the controller according to claim 24 as described above. Kikinis does not expressly disclose wherein said controller is one of the said plurality of *processors* in the multiprocessor system. The controller of Kikinis is used to control the voltage and frequency of the clocks of the other processors. Kikinis is silent with respect to the type of circuitry used within the processors. However, controllers, as is well known in the art, are often processors themselves. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the controller of Kikinis using a processor. Doing so would have allowed the controller to have excellent performance and would be programmable.

19. Claims 3 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikinis in view of Collins et al., U.S. Patent 6,157,989.

20. As to claim 27, Kikinis taught the multiprocessor system according to claim 24 as described above. Kikinis does not expressly disclose wherein the multiprocessor system comprises a single multiprocessor VLSI chip.

Collins teaches a multiprocessor system can be on single integrated circuit or may be implemented on multiple integrated circuits.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kikinis by implementing his multiprocessors on a single IC such as a VLSI chip as taught by Collins. The advantages achieved by integrating multiple processors on a single VLSI are chip are well know in the computer arts. Such advantages include: increased speed, smaller devices, reduced power and reducing cost. One of ordinary skill in the art would have made the modification for the desirable advantages.

21. As to claim 3, Kikinis taught the claimed multiprocessor system therefore he also taught the claimed method of operating it.

22. Claim 2, 15-18, 20-23 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikinis in view of Williams et al., U.S. Patent 6,397,343.

23. As to claim 26, Kikinis taught the system according to claim 24 as described above. Kikinis does not expressly teach circuitry for applying said controls to adjust operation parameters of cooling systems for said multiprocessor system.

Williams teaches circuitry for applying controls to adjust operation parameters of cooling system (cooling fans, circulation fans and the like) for a processor system [col. 9 line 64 through col. 10 line15].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kikinis by implementing the control of a cooling as taught by Williams. An artisan would have been motivated to make the modification because William teaches that implementing such a system operates efficiently allowing a range of performance to control heat generation etc. and delivers the best overall performance for the system to work without the risk of heat induced errors or damage [col. 2 lines 35-45 and col. 3 lines 66 et seq.].

24. As to claims 2 and 20, Kikinis together with Williams taught the claimed system. Therefore, they also taught the claimed method and controller.

25. As to claim 15, Kikinis taught the method according to claim 1 as described above. Kikinis teaches wherein the power and performance goals comprise data defining a desired multiprocessor power consumption level, data defining desired multiprocessor temperatures and

desired instruction execution speeds [col. 5 lines 5-41]. Specifically, Kikinis teaches that the power consumption (voltage and frequency of operation) for each processor is based it operating temperature. Kikinis does not expressly disclose wherein desired acoustic noise output, EMC levels.

As set forth hereinabove, Williams teaches desired acoustic and EMC level. For the same reasons as set forth hereinabove it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kikinis with the teachings of Williams.

26. As to claim 16 and 21, Kikinis taught the method according to claim 1 as described above. Kikinis teaches, as set forth hereinabove, wherein a set of controls comprises power supply voltage settings, clock frequency settings and operational mode settings for said processors. Kikinis does not expressly disclose cooling fan speed, controls for said system cooling means and operational mode settings for said processors.

As set forth hereinabove, Williams teaches cooling fan speeds and controls for system cooling means. For the same reasons as set forth hereinabove it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kikinis with the teachings of Williams.

27. As to claim 17 and 22, Kikinis together with Williams teach the method according to claim 16 as described above. Kikinis and Williams both teach operational mode settings comprise an active mode (working at normal operating speed and power). Both Kikinis and Williams attempt to maintain processing of data while reducing the amount of heat among other parameters within the system. The combined system would accomplish this by reducing the clock frequency, voltage and increase cooling as necessary (low power mode). Both Kikinis and

Williams also recognize damage may occur to the system as a result of critical heat buildup. One ordinary skill in the art will readily recognize that damage to the system is most undesirable result. Therefore, it would have been obvious to one of ordinary to place processors that have reached near critical temperature into a sleep power mode in order to minimize heat buildup for such processors. Doing so would prevent physical damage to the system.

28. As to claim 18 and 23, Kikinis together with Williams teach the method according to claim 16. Kikinis together with Williams does not expressly disclose wherein said cooling means comprises channeled temperature conditioned air. However, William suggests that other types of cooling apparatus would work in his system [col. 4 line 37 and col. 9 lines57-]. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the cooling system as taught in the Kikinis and Williams to use channeled temperature conditioned air. One of ordinary skill would have recognized that using channeled temperature conditioned air would have a greater cooling effect that just using a fan alone. This cooling effect is desirable in the system of Kikinis together with Williams.

29. Claims 4-6, and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikinis and Collins in view of Williams.

30. As to claim 28, Kikinis together with Collins taught the multiprocessor system according to claim 27. Kikinis together with Collins does not expressly disclose wherein the multiprocessor system comprises a cooling means for said multiprocessor VLSI chip.

Williams teaches a system having a cooling means for a processor system [col. 9 line 64 et seq.].

It would have been obvious to one of ordinary to modify Kikinis together with Collins by implementing the cooling means for a processor system as taught by Williams. One of ordinary skill in the art would have expected the cooling system of Williams to work with the system of Kikinis and Collins. One of ordinary skill would have made the modification because Williams teaches that his cooling system would desirably the system to work without heat induced errors or damage without the loss of performance [col. 2 lines 35-45 and col. 3 lines 66 et seq.].

31. As to claim 29, Kikinis together with Collins and Williams taught the multiprocessor system according to claim 29. Williams further teaches wherein the cooling means comprises a single chip cooling fan [col. 9 lines 64-66].

32. As to claims 4 and 5, Kikinis together with Collins and Williams taught the multiprocessor system. Therefore, they also taught the method of operating it.

33. As to claim 6, Kikinis together with Collins and Williams taught the multiprocessor system according to claim 4 described above.

Kikinis together with Collins and Williams do not expressly disclose wherein said cooling means comprises a controllable single chip thermo-electric cooler.

However, William does suggest that cooling means (other cooling apparatus) other than a fan may be used [col. 4 lines 35-38].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kikinis together with Collins and Williams by implementing a thermo-electric cooler as a cooling means. Thermo-electric coolers are well known is the art for cooling a processor. One of ordinary skill would have recognized that a thermo-electric would also allow active

cooling of the system and can be used in place of or in addition to a cooling fan for the purpose of cooling the chip.

34. Claims 7-9 and 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikinis together with Collins and in further view of Williams and applicant's admitted prior art (AAPA).

35. As to claim 30, Kikinis together with Collins taught the system according to claim 27, described above. Kikinis together with Collins teaches a multiprocessor system comprising a self-contained multiprocessor system.

Kikinis together with Collins does not expressly disclose said multiprocessor system comprising a plurality of multiprocessor VLSI chips, and said self-contained multiprocessor system further comprising a first controllable cooling system.

Williams teaches as system where the cooling system is a controllable cooling system.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kikinis together with Collins by implementing the cooling system as taught by Williams. One of ordinary skill would have made the modification because Williams teaches that his system allows the system to function at maximum performance without increasing the risk of heat induced errors or damage [col. 3 lines 41-45 and col. 9 lines 64 et seq.]. One of ordinary skill in the art would have expected that the teachings of Williams would be successful in the multiprocessor system of Kikinis and Collins.

AAPA teaches a system having a plurality of multiprocessor VLSI chips [page 4 lines 3-14]. It would have been obvious to one of ordinary skill in the art at the time of the invention to

modify Kikinis, Collins and Williams by implement their teachings into the environment of AAPA. One of ordinary skill in the art would have reasonable expectation that their system would be successful in the environment of AAPA to achieve the advantage of maximizing the performance.

36. As to claim 31, Kikinis together with Collins, Williams and AAPA taught the system according to claim 30. AAPA further teaches wherein the multiprocessor system comprises a rack multiprocessor system comprising a plurality of said self-contained multiprocessor systems and rack cooling system [page 2 lines 4-16 and page 4 lines 3-14]. Williams teaches that the cooling system would be controllable.

37. As to claim 32, Kikinis together with Collins, Williams and AAPA taught the system according to claim 31. AAPA further teaches wherein said multiprocessor system comprises a plurality of said rack multiprocessor systems [page 4 lines 3-14]. Williams teaches that the cooling system would be controllable cooling means.

38. As to claims 7-9, Kikinis together with Collins, Williams and AAPA taught the claimed system therefore they also teach the claimed method of operating the system.

39. Claims 10 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikinis in view of Williams, Vladimir, U.S. Patent 6,639,883 and Lewis et al. U.S. Patent 5,906,315.

40. As to claim 10, Kikinis taught the method according to claim 1 as described above. Kikinis teaches wherein first sensor data comprises temperatures of said processors in said multiprocessor system [col. 4 lines 23-32]. Kikinis further teaches that the clock frequencies and

the supply voltage corresponding to circuits must be detected as part of the first sensor data [col. 5 line 29-41].

Kikinis does not expressly disclose wherein the data comprises, electromagnetic radiation of the multiprocessor system, acoustic levels of said multiprocessor system, vibration levels of said multiprocessor system, and air temperature of cooling system in said multiprocessor system.

Williams teaches using sensor data that comprises electromagnetic radiation (EMI) and acoustic levels of a processor system [col. 9 lines 46-63].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kikinis by also implementing the sensor data as taught by Williams as part of the first sensor data. One of ordinary skill in the art would have made the modification because it would allow both noise and EMI to remain within at desired levels.

Vladimir teaches using monitoring vibration levels using sensor data within a computer system [col. 3 lines 16-19 and col. 4 line 66 through col. 5 lines 24]. Vladimir then determines if the vibration levels exceed an allowable level and if so adjusts the rotation rate to reduce the vibration.

It would have been obvious to one of ordinary skill in the art at the time to modify Kikinis by implementing the sensor data comprising vibration levels as taught by Vladimir as part of the first sensor data. One of ordinary skill would have made the modification because Vladimir teaches that his method would reduce the main source of undesirable vibration in a computer system. This reduction of vibration would also be desirable in Kikinis.

Lewis teaches sensor data comprising air temperatures of cooling system [col. 4 lines 16-32]. Lewis uses the air temperature data to prevent the computer system from overheating.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kikinis by implement the sensor data comprising air temperature of cooling systems as part of the first sensor data. One of ordinary skill would have made the modification because Lewis teaches that using the air temperature would prevent the computer systems from overheating.

41. As to claim 14, Kikinis taught the method according to claim 12, as described above. Kikinis does not expressly disclose wherein the policy of operation parameters comprise defining a cost of power, acceptable acoustic noise level data, acceptable EMC output noise level data, acceptable output vibration level data, and acceptable temperature level data for the elements of said multiprocessor system. However, for the same reasons as set forth hereinabove in the rejection of claim 10, claim 14 is also rejected. Additionally, Williams teaches defining a cost of power [col. 3 line 35 through col. 4 line 11]. Specifically, Williams discloses this system provides the best overall performance to a user. The system of Williams would operate efficiently allowing maximum performance while at the same time adjusting the adjusting the heat output without reducing the system capabilities.

Conclusion

42. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 6,718,474 to Somers et al. This patent teaches a method and apparatus for clock management based on environmental conditions.

U.S. Pat. No. 6,560,658 to Singer et al. This patent teaches a system with a data storage device which has reduced mode of vibration.

U.S. Pat. No. 6,119,241 to Michail et al. This patent teaches a system and method that self regulates processing based on temperature.

U.S. Pat. No. 6,000,036 to Durham et al. This patent teaches a system with a plurality of processors that steers instructions from processing regions that are too hot.

U.S. Pat. No. 5,881,298 to Cathey. This patent teaches a computer system that uses a thermo-electric cooler.

U.S. Pat. No. 5,484,012 to Hiratsuka. This patent teaches a computer system that changes fan speed based on monitoring of the ambient.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (703) 308-6291. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (703)308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James Trujillo
April 27, 2004

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER ~~2600~~ 2100